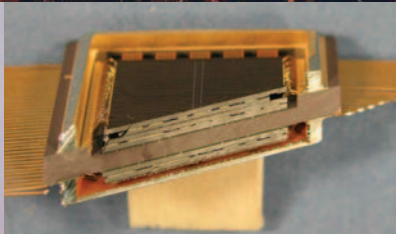
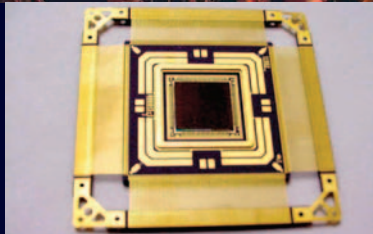
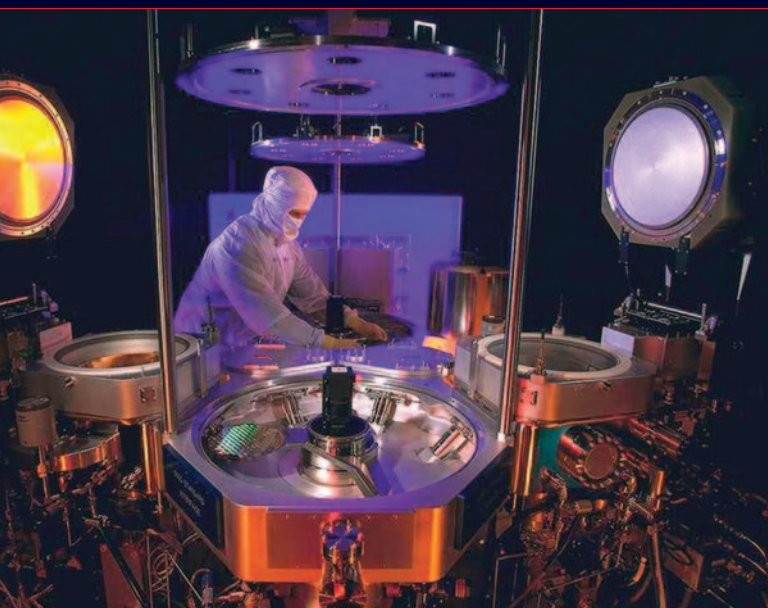


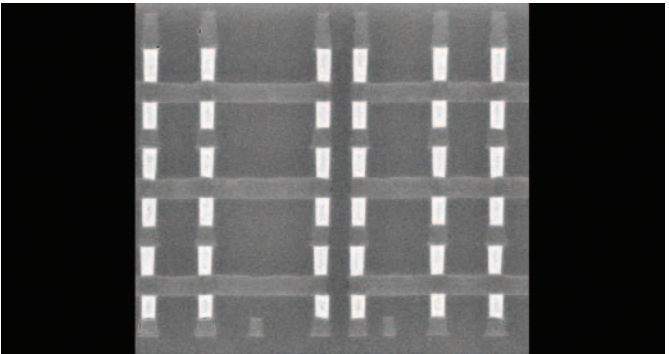
# Flexible Foundry and Design Services



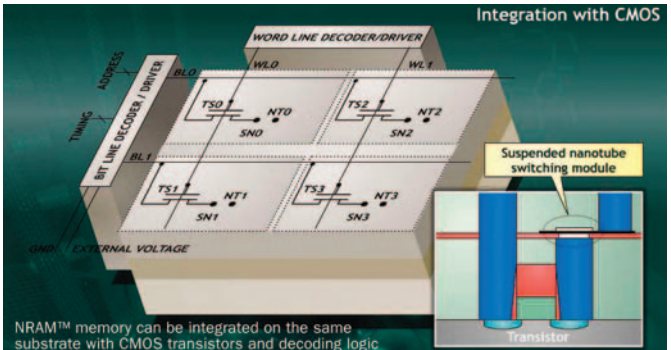
# Fab diversification

For the past 25 years, the Semiconductor Technology Center has adapted several generations of commercial technologies to specific applications and has developed its own IP to extend the capabilities of traditional CMOS to unique environments, licensed IP for specialized applications such as Anitfuse technologies, non-volatile memory technology and is investigating the implementation of Carbon Nanotube technology, SiGe BiCMOS, photonics, MEMS, and copper interconnects. In addition, the Semiconductor Technology Center has worked with many companies to bring to market its new IP and concepts, using BAE Systems state-of-the-art tools and expertise, all in a confidential environment to protect their competitive edge.

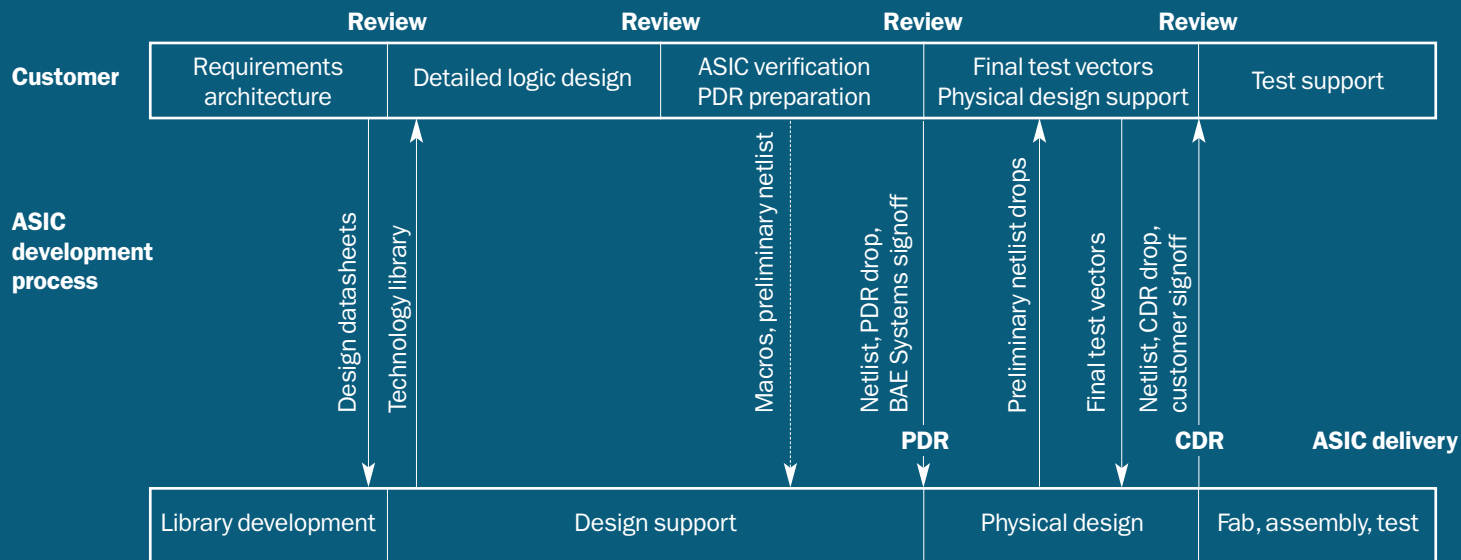
## 7-level metallization



## Carbon nanotube device (courtesy of Nantero, Inc.)



## Typical “netlist-entry” ASIC design process



Standard commercial EDA software tools, up to 15 Mgates

## Packaging

Qualified flip chip and wirebond production

Double-sided C4/wirebond memory stack

Qualified production of MCMs

- Stacked double-sided ceramic

- Flip chip/wirebond connection

- Logic/memory devices

- Analog /digital modules

Qualified Ceramic Column Grid Array (CCGA)

- High rel /high performance

- 500+ signal I/O

- SMT board compatibility

Plastic Ball Grid Array (BGA)

- Wirebond/flip chip

- Low weight/high performance

## Test capabilities

High speed /high pin count logic & memory testers

Diverse test program development experience:

- ASICs, Processors, FPGAs, SRAMs, PROMs, FIFOs, SDRAMs

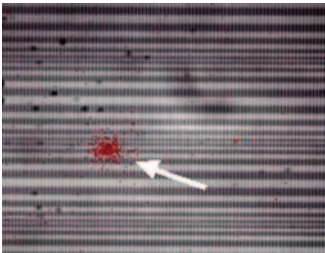
Extensive experience with design for testability techniques

Up to 8" wafer test with hot chuck using known good die test techniques

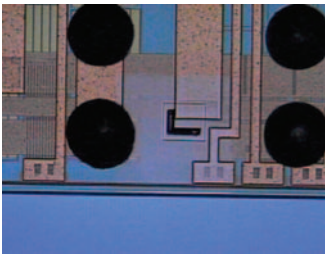
Full mil temp packaged part testing

# Failure analysis

The Failure Analysis Laboratory has unique experience in analyzing heritage technologies such as flip-chip, MCM and planarized devices. Root cause analysis to determine if the fault is a design, manufacturing defect, or an induced failure is routinely performed on VLSI devices. The laboratory has a Focused Ion Beam System with SIMS capability that is critical for VLSI Design debug and repair, as well as process characterization. The laboratory has a “backside” Photoemission Microscopy capability for finding defects under dense interconnect layers or on flip-chip devices. These and many other available instruments are essential for fault diagnostics of ASIC, SRAM, CCD, ROIC, Processors, and Sensor devices. Microscopic Cross-sections are processed and investigated with a Hitachi S-4800 Field Emission SEM capable of 800,000X magnification. Material analysis is performed using an EDAX Phoenix Energy Dispersive Spectroscopy. EDS enables elemental analysis down to Boron. Reports are disseminated electronically.



**A photoemission image of a defect observed through the backside of a flip chip device**



**ASIC prototype requiring a FIB patch with an opened window, isolation and platinum deposition**

## Aracor xray irradiator



## Semiconductor Technology Center

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The BAE Systems Semiconductor Technology Center (STC), Manassas, Virginia, has been providing products and system solutions to the commercial and space community since the early 1980s and is continuing this tradition with the current 0.25  $\mu\text{m}$  CMOS process in 2004 and the 0.15  $\mu\text{m}$  CMOS process installation in 2005. The STC is a world leader in the manufacture of qualified space level semiconductor devices with advanced wafer fabrication equipment. Current and planned products include radiation-hardened 4Mb SRAM, 4Mb Nonvolatile Memory, RAD750 microprocessor, 250K gate FPGA, Read Out Integrated Circuits and high density ASICs. Extensive capability exists to implement low to medium volume product development and production with special/unique process recipes and novel materials.

In addition to the wafer manufacturing facility, we have packaging, military screening, testing, and other supporting facilities. STC offers a broad selection of cost-effective, space-qualified technologies for high-density packaging to meet high-performance application needs. We have fully equipped VLSI characterization, failure analysis and reliability laboratories that carry out routine and diagnostic testing and evaluation. We also have strong expertise in semiconductor design for memory and ASIC products complete with the latest tools.

# Facilities

Semiconductor fabrication facility 49,466 sq. ft.

Main facility (class 100) 19,396 sq ft

QML qualified production of microprocessors, ASICs, and memories (rad hard, space/mil) development, and manufacturing of advanced technologies as needed

Advanced lithography facility (class 1) 5,540 sq. ft.

0.25  $\mu\text{m}$  lithography with 200 nm overlay  
0.15  $\mu\text{m}$  image with 60 nm overlay capability

Advanced back-end-of-line facility (class 10) 5,378 sq. ft.

Planarized interconnection process using chemical-mechanical polishing for oxides and metals

Packaging facility 6,520 sq. ft.

QML qualified flip chip, wirebond, and MCM assembly processes

Semiconductor test facility 6,219 sq. ft.

Memory: Teradyne J937 testers, GSI M325 laser system  
Logic: Advantest testers (T3382, T3340, T6682)

Semiconductor screening facility Reliability 1,955 sq. ft.,  
Failure analysis 2,688 sq. ft, Burn-in 1,770 sq. ft.

Full military screening capability. ARACOR x-ray irradiator and J.L. Shepherd model 109-68 Cobalt 60

Board assembly and test facility 2,223 sq. ft.

Space qualified board assembly, functional test, cleaning and coating

Systems/subsystems integration

Systems/subsystems assembly, software integration, functional and environmental test

BAE Systems currently has a 50,000 sq. ft. manufacturing process facility in Manassas, Virginia. The Semiconductor Technology Center contains a Class 100 main facility, a Class 1 Advanced Lithography facility, a Class 10 Back End of Line (BEOL) area, a Class 100 module assembly lab, and test and mil-screening areas. Our packaging facility has wire bond, C4 flip chip and column grid array (CGA) capability.

Recent upgrades to this facility include the acquisition of state-of-the-art tools. Highlights of this modernization activity are a new ASML Deep UV scanner, Applied Materials Centura/Endura and Akron wet stations.

For further information contact:  
BAE SYSTEMS  
Information & Electronic Warfare Systems  
9300 Wellington Road  
Manassas, VA 20110-4122  
Telephone 1-866-530-8104  
[www.iews.na.baesystems.com/space](http://www.iews.na.baesystems.com/space)