

# MAGNUM 4 Mb radiation-hardened SRAM

## MAGNUM FAMILY OF PRODUCTS

MAGNUM is our third generation of 3.3V radiation-hardened 4M SRAM and has been designed to withstand the effects of natural space as well as a radiation-hardened environment.

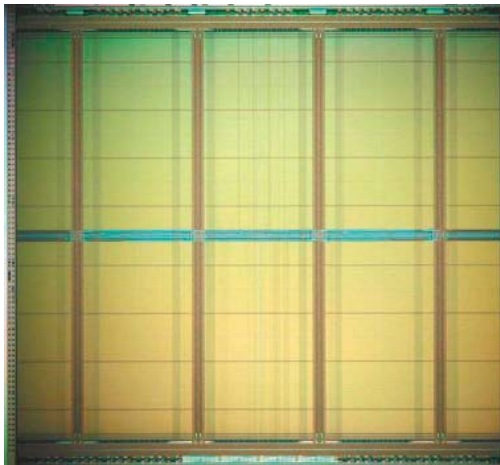
4 Mb single-chip, up to 16 Mb multi-chip module packages available

512K x 8 SRAM  
– 40 lead flatpack

512K x 16 SRAM  
– 64 lead flatpack

1M x 16 SRAM  
– 64 lead flatpack

512K x 32 SRAM  
– 84 lead flatpack



## FEATURES AND CAPABILITIES

Standard microcircuit drawing #5962-07210

QML compliant part

Read/write access times of 25-30 ns

Single 3.3V  $\pm$  10% power supply

Standby current 5-15 mA

Operating temperature range -55° C to 125° C

Asynchronous operation

Operating power < 23 mW per MHz

Radiation levels

- TID >  $1 \times 10^6$  rad (Si)
- SEU <  $1 \times 10^{-10}$  bit/day (90% Geo)
- Prompt dose upset >  $1 \times 10^9$  rad (Si)/s
- Prompt dose survival >  $1 \times 10^{12}$  rad (Si)/s
- Neutron fluence >  $1 \times 10^{13}$  n/cm<sup>2</sup>
- Latch-up immune

**SYSTEM DEFINITIONS**

A:0-18 Address input pins that select a particular eight-bit word within the memory array.

DQ:0-7 Bi-directional data pins that serve as data outputs during a read operation and as data inputs during a write operation.

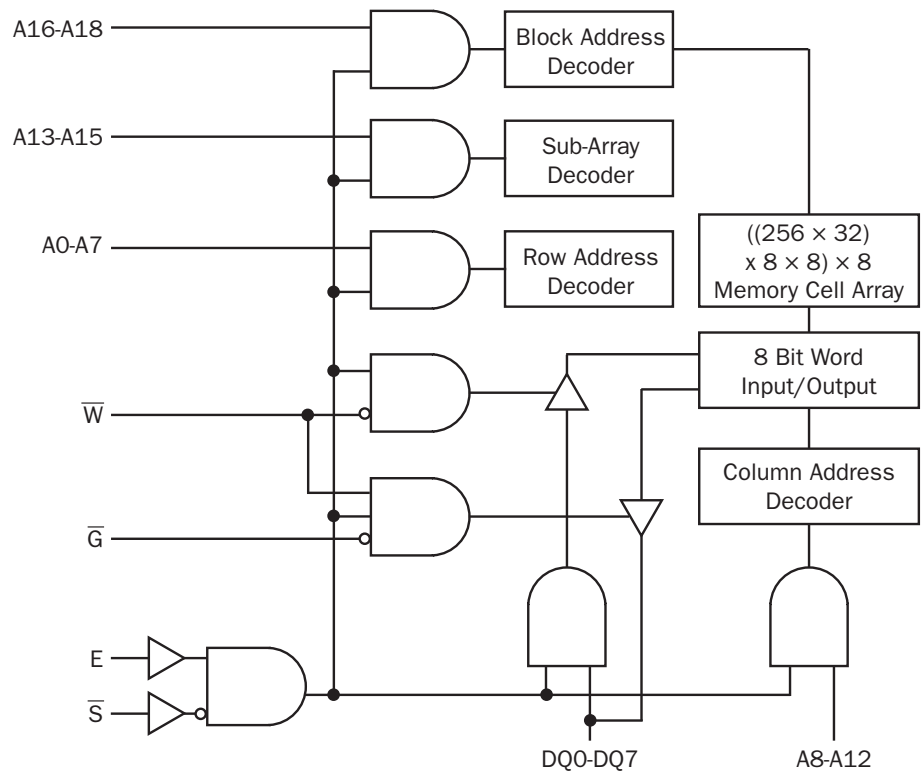
$\bar{S}$  Negative chip-select, when at a low level, allows normal read or write operation. When at a high level,  $\bar{S}$  forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables the data input buffers only. If this signal is not used, it must be connected to GND.

$\bar{W}$  Negative write-enable, when at a low level, activates a write operation and holds the data output drivers in a high-impedance state. When at a high level,  $\bar{W}$  allows normal read operation.

$\bar{G}$  Negative output-enable, when at a high level, holds the data output drivers in a high-impedance state. When at a low level, the data output driver state is defined by  $\bar{S}$ ,  $\bar{W}$ , and  $\bar{E}$ . If this signal is not used, it must be connected to GND.

$\bar{E}$  Chip-enable, when at a high level, allows normal operation. When at a low level,  $\bar{E}$  forces the SRAM to a precharge condition, holds the data output drivers in a high-impedance state, and disables all the input buffers except the  $\bar{S}$  input buffer. If this signal is not used, it must be connected to  $V_{DD}$ .

**FUNCTIONAL DIAGRAM**



**FOR MORE INFORMATION, CONTACT:**

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