Characterization of the 4Mb Chalcogenide-Random Access Memory

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Abstract-- **The first generation of C-RAM memory is designed to greatly exceed (in density, write speed, endurance) the existing non-volatile memory solutions for space and to close the gap that exists between system requirements and availability. Based on the success of the 64kb C-RAM program, a 4Mb C-RAM prototype has been designed and fabricated in 0.25 μm radiation-hardened CMOS. In this paper we present a description of the 4Mb design as well as results of recent characterization and radiation test of the first pass of prototype parts.**

Index Terms—**Chalcogenide, phase change, nonvolatile, memory**

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I. INTRODUCTION

PHASE-CHANGE nonvolatile memories are emerging as one of several viable candidates for the next generation of solid state non-volatile memory products. Most commercial research is focused on the chalcogenide material ($Ge_2Sb_2Te_5$) used for rewritable optical media (CD-RW and DVD-RW) [1]. This alloy is the product of a long material development effort, starting in 1968 [2]-[5]. Investigations into its suitability for solid-state applications as well as optical products provided optimism that memory devices could be economically produced that might rival or even surpass existing solid-state memory - both nonvolatile and volatile [6]-[8].

Commercial interest in phase-change memories accelerated in 2000, and now includes separate developments in Ovonic Unified Memory (OUM) and Phase-change Random Access Memory (PRAM) at Intel [9]-[11], ST Microelectronics, Samsung [12]-[16], and Hitachi [17].

The Air Force Research Laboratory initiated a program in 1999 to research and develop chalcogenide technology for space applications. The Chalcogenide-based Random Access Memory (C-RAM™) program combines the phase-change expertise of Ovonyx, Inc. with the radiation hardened CMOS processing capability of BAE SYSTEMS [18], [19] to focus on a radiation-hardened, fast, low-power, high-endurance nonvolatile memory. The initial demonstration phase produced 64kb memory arrays on radiation hardened 0.5 μm CMOS technology and showed no total dose or single event degradation to the hardened CMOS or effects that can be attributed to the phase-change material [20], [21].

Results from our 64kb test chip have been presented in prior NVMTS papers [24], [26]. The results reported demonstration of an array of chalcogenide memory characterized for radiation environments and temperature that allowed us to transition the 64kb building block to 0.25μm technology and replicate with support circuitry to design and demonstrate a 4Mb memory.

The following sections will discuss the 4Mb C-RAM design and early results from hardware characterization and radiation test.

II. 4MB C-RAM DESIGN FOR TESTABILITY

The goal of the 4 Mb C-RAM prototype program is to demonstrate a fully functional product and to provide sufficient measurement feedback on the material performance and internal circuit elements. Special features are incorporated in the design to determine the margins associated with programmed SET/RESET resistances, the optimum write currents and read voltages. In addition, analog variations of the write current and external override of read voltage are provided for characterization of the chalcogenide process.

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Because this is a prototype design, the amplitude and pulse widths of the Write 1 and Write 0 circuits have been designed to be variable based upon pad-selectable digital inputs that can be modulated at wafer test. These selection inputs can be used to determine optimal settings for the write pulse generator circuit on a per-chip basis and can also be varied to characterize parametric trade-offs affecting write cycle endurance, data retention time and overall product reliability. This data will be fed into future designs to reduce complexity and production test time and to improve manufacturability and device reliability. The optimized selection will be "locked" into each prototype die by laser implemented programming fuses prior to packaging.

To ensure reliable operation of each 4Mb C-RAM die it will be necessary to determine the margin between the programmed SET/RESET resistances and the switching resistance of the sense amplifier circuitry used to read the state. Anomalous bits with programmed resistance values very close to the sense amplifier switching resistance may pass initial testing, but subsequently fail due to small variations in programmed resistance values. To be able to identify these devices during test, the 4Mb C-RAM has been designed with an analog input that controls the amount of current through the reference resistor in the sense amplifier, changing the effective switching resistance. Varying the voltage level on this input and monitoring the number of bit fails will allow for determination of the margin between the switching resistance and the programmed resistance of bits in the memory array. During normal operation this input will be tied to V_{DD}. Once the programmed resistance values have been mapped using this procedure, a digital trimming option will be invoked that will optimize the switching resistance. This is accomplished by switching in transistors that modify the gain of the current mirror used to amplify the current through the reference resistor.

To aid diagnostics, the part is also capable, with a single mask change, of being operated as a 256kb x 8 (2 Mb total) device, where two cells are written and read for each logical bit. This mode will be used to compare device stability between the single and double cell options. Additional mask-programmed changes are available to diagnose additional circuits, including the band-gap reference used to stabilize the write amplitude across temperature and voltage variations.

III. 4Mb C-RAM Characterization

Characterization of the CRAM was done at various assembly levels. Wafer level testing was used as an initial look at the memory functionality and to determine optimal trim settings. More extensive testing was then performed on die assembled into a 40-pin ceramic flat pack previously used for 1Mb SRAM products. Additionally, to provide further insight into the relationship between the various digital and analog trim values vs. performance, some die were mounted onto a 172 pin quad flat pack.

Typically, the prime objective of wafer level testing is to simply identify those die which are worth packaging into modules. Wafer testing can only be performed at a reduced temperature range, and provides an electrical environment that is significantly worse than the die will encounter at higher levels of assembly due to probe inductance, contact resistance, etc. Furthermore, for die that will be wire bonded, each contact of the probes to the product tends to degrade wire bondability, as the scrubbing action of the probes onto the chip pad, necessary to remove oxide and ensure good electrical contact, tends to damage the chip pad and can only be repeated a limited number of times.

CRAM wafer testing was further complicated by the requirement that the optimal trim setting for each die be determined and laser fused for product being packaged into the 40-pin package. Four aspects of CRAM operation were selectable: the write current amplitude (8 settings possible), the Write 0 pulse width (2 settings), the Write 1 pulse width (4 settings), the Sense Amp Set Point (4 settings), and adjustments to the Write Compensation Circuitry (8 settings). The sense amp set points could be further modulated in an analog manner by varying Vdd_Ref , and the write current could modulated by Vdd_WH (Write Head).

The need to provide as early as possible feedback on CRAM functionality to the design and process community, plus the trim setting requirements significantly exceeded the capabilities of the standard memory test software and production automated test equipment (ATE). This was solved by the development of a software suite which uses a control and command structure to explicitly define what tests are to be applied to a single die on a wafer and under what conditions. It included the ability to vary isolated trim parameter (e.g., Sense Amp Set Point) in a restricted manner, while holding other trim parameters (e.g., Write Amplitude) fixed, and, in turn, recording the extent of failures observed. The results of each test suite can then be passed on to subsequent test suites thus linking local optimizations into a global solution that has been developed on each individual die.

For each evaluated trim setting, the test was performed three times, once testing only for zeroes (ignoring the response when a one was expected), testing only for ones (ignoring expect zero), and testing normally (expect zeroes and ones). This capability was quite useful in isolating the effect of the trim settings on reading/writing zeroes vs. reading/writing ones.

The combination of trim circuitry, isolation of the Sense Amp reference voltage (Vref), and testing of zeroes independently of ones, permits the development histograms which can estimate the set and reset distribution of the 4Mb of memory cells. This analysis can be performed at various stages to assess the effect of testing, stressing, etc., on the full population of bits.

Cell resistance is typically lowest immediately after completing processing, prior to testing, in its so-called Virgin State [10]. Performing a read, expecting a one (set state), revealed that, for good die, virgin resistance was consistently below the lowest SA setting (15kΩ), as expected.

Prior experience, both from discrete device characterization and C-RAM test chip fabrication [26] have established the value of preconditioning memory bits prior to manufacturing test. The prime benefit of this operation is to improve the distribution of Rreset, as can be seen from Figure 1, taken from discrete devices. These figures demonstrate a modest improvement in Rset as well. Preconditioning is performed by raising Vdd above its standard range, and elongating the write pulse width.

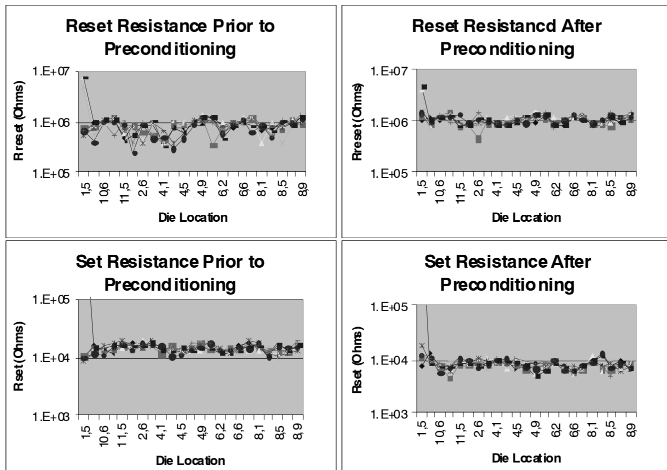

Figure 1. Affect of Preconditioning on Pass 1.0 die

Performing similar preconditioning on Memory Die is more challenging, however. Even with the availability of trimming and write current (V_WH) adjustments, the embedded nature of the bit cell, and self timing circuitry reduced the effectiveness of this step.

However, even without an optimized preconditioning, the tested wafers showed a high degree of functionality. Adequate set vs. reset resistance was achieved across the entire die, as shown, in Figure 2. Subsequent wafer level testing on both 2Mb and 4Mb die revealed a number of die with 99.9%+ functional bits, prior to repair. These die were then packaged into the 172 and 40 pin packages for further evaluation.

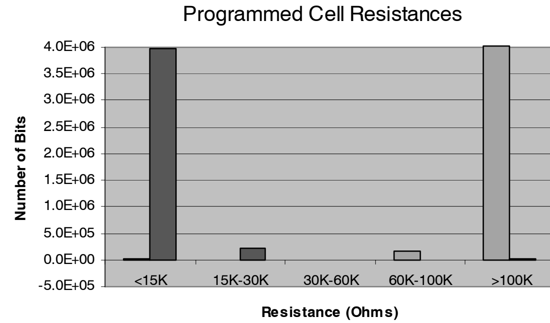

Figure 2. Distribution of programmed resistances

IV. 4MB C-RAM RADIATION TESTING OVERVIEW

The goals of radiation testing are to verify that the device meets the minimum radiation hardness requirements outlined in Table 1.

Table 1
4M CRAM Program Goal and Test Hardware Parameters

Parameter	Requirement
Size &Architecture 0.25 micron technology	4M CRAM 512K x 8
Total Ionizing Dose - (rd(Si)) (4)	≥ 1Mrd(Si)
Single-Event-Upset - (errors/bit-day) (1)	< 1E-11
Single-Event-Latchup - (LET in Mev-cm^2/mg) (2)	> 120
Dose-Rate Upset - (rd(SiO_2)/s) (3)	≥ 1E9 Rd (SiO_2)/s

(1) Adams 10% Worst-Case environment under worst-case operating conditions for voltage, temperature and memory operating conditions (e.g., static or dynamic operation).
(2) Under worst-case voltage and temperature operating conditions.
(3) Dose-rate testing shall be accomplished using a 20 to 50 ns FWHM pulse, under worst-case voltage and temperature operating conditions, for both static and dynamic operation. The operation of the device-under-test shall be monitored for memory cell upset, I/O upset defined as a voltage excursion > Vdd/3 and any access time push-out.
(4) Testing shall be done IAW MIL-T-1019.5 using a Cobalt-60 source at a dose-rate between 50 to 300 rd (Si)/s.

For this paper, the results of prototype SEE and Prompt Dose evaluation will be presented

A. Test Equipment

The test apparatus will consist of a Device Under Test (DUT) test card and tester which is used to provide all stimulus and sample interrogation during testing. A standard test setup is shown in Figure 3. Each DUT card will be custom to ensure ample signal integrity and noise decoupling during testing. The stimulus during TID testing will come from a compact Mosaid Systems MS2200 Portable Memory Test System. This unit will be used to provide all bias and stimulation while in the gamma source. Additional characterization testing will be done remotely, using an IMS XTS Blazer tester. Prompt Dose and SEE testing will be done using another Mosaid Systems tester, the MS3490. This tester will provide the capability real time bit mapping along with increased test speed (20 MHz performance, with the capability of 16X and 16Y address depth and 18 I/O). In addition, power supply sensing and current monitoring during all tests will be accomplished with the aid of a host of Agilent Digital Multimeters, and Power supplies.

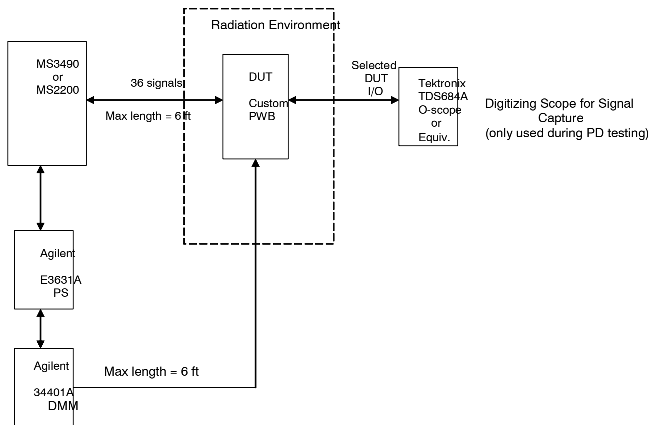

Figure 3. Standard Test Apparatus Diagram

B. Single Event Effects (SEE)

1) SEE Evaluation

SEE evaluation of the prototype 4M array was performed on May 30, 2005 and July 29, 2005 at the Lawrence Berkeley National Laboratory. The following test scenario was followed:

The five 4Mb C-RAM devices were irradiated by the Lawrence Berkeley National Laboratory 88-inch Cyclotron with ion attributes of minimum range (in Silicon) of 30 um, delivering Effective LET ranging between 1.5 MeV/mg/cm2 and 120 MeV/mg/cm2. An LET > 60 MeV/mg/cm2 was obtained using > 0 degree incident angles. A beam flux of between 1E4 and 1E5 p/cm2/s to a maximum fluence of 1E7 p/cm2 was obtained.

The voltage across the devices was nominally 3.3V, with a VDD of -10% (3.0V) for upset testing and +10% (3.63) and +20% (3.96) for latch-up testing. Upset testing was performed at nominal operating temperature or 25ºC. Latch-up testing was performed at maximum operating temperature, 125ºC.

A Core Memory Test Pattern of all 1's, all 0's, and Checkerboard (by address to create physical checkerboard) was written to the devices under test. Prior to beam exposure, each sample underwent a functional characterization at the temperature designated for the evaluation.

The static upset test consisted of an "operable" test where the supply voltage was maintained throughout the entire exposure and a "non-volatile" test where the supply was removed during exposure.

The static operable upset test consisted of the following:

(1) Pre-write and verify of the memory pattern prior to exposure. (Build Mask)

(2) Part exposure, while powered with core memory pattern maintained

(3) Post exposure readout and verification of corrupted memory locations which is logged along with address location to further isolate array sensitivities. The absence of latch-up was also verified.

The static "non-volatile" test was similar to the operational test, except during exposure the part was un-powered.

The stored memory pattern was a physical checkerboard pattern. The test was performed at VDD=3.0V, and Tcase = 25ºC. The particle fluence for this exposure was 1E7 p/cm2.

Dynamic read upset testing was performed at the same VDD supply and case temperature as the static test. The dynamic read upset test consisted of the following:

(1) Pre-test write-read of the device to verify functionality prior to beam exposure. (Build Mask)

(2) Part-placed in a continuous read test loop with verification of no errors prior to beam turn-on.

(3) Beam exposure of the device while continuously reading an logging cumulative fail count (no address logging during this test)

(4) Stop beam and verify that error count ceases (verify no permanent damage to part due to latch-up)

The same particle fluence and fail count attributes applied as in static testing.

In addition to upset tests, latch-up test was performed using the dynamic operational test procedure with supply voltage changes to VDD= VDD nominal + 10% and 20% (3.63 V and 3.96V) and the test temperature at 125ºC. Sample functionality and VDD supply current was monitored to check for the absence of latch-up. Latch-up testing was done up to maximum effective LET, which took into account angular dependence of the incident ion.

2) SEE Results

As shown in Figure 4, the C-RAM prototype part exhibited small numbers transient bit errors (read 0, expecting 1) during the static testing sequence. The transient nature of these errors indicated that the C-RAM bit was not affected by the beam particles.

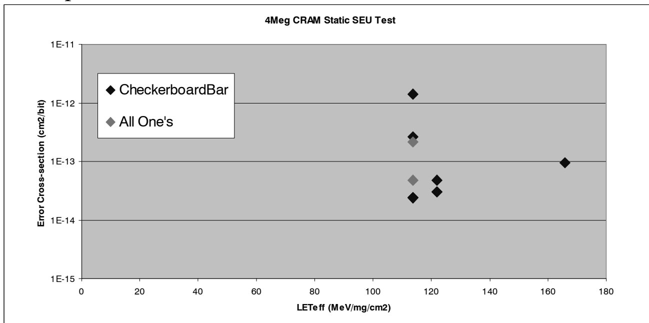

Figure 4. SEE Test Results (Static Read)

At present, analysis is underway to identify the root cause of the transient errors before the release of the pass 2 design. Since the Sense Amp and the Reference Voltage Circuits are known to be sensitive in the Pass 1 prototype, the current analysis is focusing on those areas.

Two problems were identified in the early dynamic read SEE testing of the 64kb array. The first problem involved an SEE induced turn on of write circuitry with resulting memory bit corruption. An additional transient read upset was also observed, but with no permanent corruption of the memory bit. The first pass 4M prototype part contained a design enhancement to eliminate the first upset condition. Pass 2 of the design will correct for the second condition as well.

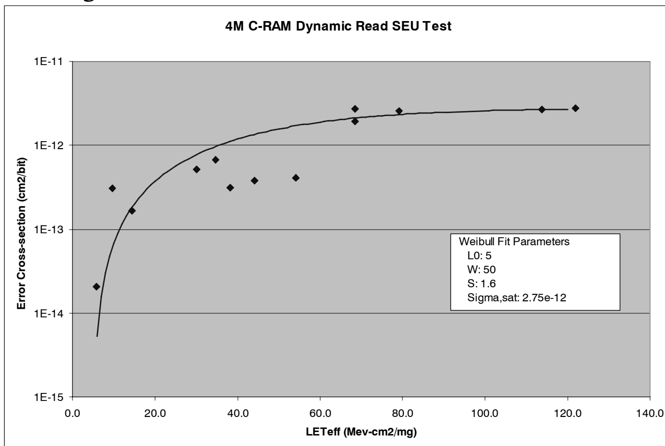

Figure 5. SEE Test Results (Dynamic Read)

Figure 5 contains the results from the Dynamic Read SEE evaluation. In every case, errors returned to 0 when the part was removed from the beam. An upset rate of 2E-12 upsets/bit-day was calculated using the observed cross section and LET for a 90% WC Geo orbit.

Surprisingly, the NV test yielded errors consisting of permanently altered bits. These errors included, in one case, all 8 bits of multiple addresses. Further analysis revealed, however, that the errors were due to repeatable (off beam) tester induced voltage conditions during the power sequencing procedure. Analysis of the exact failure mechanism will be completed prior to the Pass 2 release.

Finally, the parts were observed to be latch-up immune to the maximum effective LET available at the test facility (141.2 MeV/mg/cm2).

Burnout testing was performed using the Hermes III Flash X-ray located at the Sandia National Laboratory (Bremsstrahlung mode).

C. Prompt Dose Upset

1) Prompt Dose Upset Evaluation

Dose rate upset characterization testing was performed at the Boeing Radiation Effects Laboratory (BREL) using a 10 MeV linear electron accelerator (LINAC).

Based on the primary cause of device failure in most CMOS circuits (large photo current induced power supply collapse), a custom circuit board was required for this test to minimize lead inductance. The test particulars follow:

The 4Mb C-RAM devices were irradiated by the Boeing Radiation Effects Laboratory LINAC. The LINAC is capable of dose rates between 1E6 and 1E10 rd (Si)/s with pulse widths ranging between 20 nS and 1 uS.

The voltage across the devices was nominally 3.3V, with a VDD of -10% (3.0V) for upset testing. Upset testing was performed at nominal operating temperature or 25ºC.

A Core Memory Test Pattern of electrical checkerboard (by address and data word) was written to the devices under test. Static and Dynamic operational tests were performed, with data outputs resistively loaded for maximum I/O current during exposure.

For the static test, the pulse width was confined to a range of 20 ns to 50 ns. This width was measured and documented using a calibrated PIN diode and is based on the Full Width Half Maximum (FWHM) of that waveform.

The pulse was synchronized to the operational cycle of the device for the dynamic test procedure. During the dynamic test, the pulse was "walked" through the entire read and write functional cycles.

Both static and dynamic testing were conducted using a Mosaid MS3490 Memory Test System.

The static test flow and bias conditions mimicked those used during static heavy ion upset testing. The few differences are outlined below.

(1) During exposure I/O transients were monitored on I/O driving low and high voltage levels (I/O will be resistively loaded to simulate maximum load fan-out).

(2) Dose rate was varied between 1E8 and 1E10 rd(Si)/s

(3) At each dose rate the device was monitored for a change in core storage state and I/O transient response

(4) I/O transient fail was defined to be a value ≥ (Voh-Vol)/3

Dynamic write and read tests were performed separately to determine the ability of the CRAM to operate through a prompt dose event. The dynamic test flow is as follows.

Dynamic Write Upset Test Flow:

(1) Pre-exposure verification of device functionality was performed (e.g. write specific exposure pattern into then verify it's content and build mask)

(2) Tester conditioned to wait for a trigger from LINAC to start execution of a write to memory

(3) Immediately following each exposure, a read of the device was executed to determine the number of core failures and their locations, if any (this will provide further insight into the nature of the write failure)

Dynamic Read Upset Test Flow:

(1) Pre-exposure verification of device functionality was performed (e.g. write specific exposure pattern into then verify it's content, build mask)

(2) Tester conditioned to wait for a trigger from LINAC to start execution of a read from memory

(3) Immediately after exposure, the tester error counter was interrogated to look for transient errors during the actual read. A subsequent read was then performed to look for "hard" cell failures. (e.g. flipped cells)

(4) The number of transient and hard cell failures were recorded.

(5) This test was conducted over the same dose rate range as the static test.

2) Prompt Dose Upset Results

No permanent bit errors (flipped bits) were observed during static or dynamic testing of the C-RAM prototype results. However, an output transient (Figure 6) was observed during both static testing and dynamic read testing.

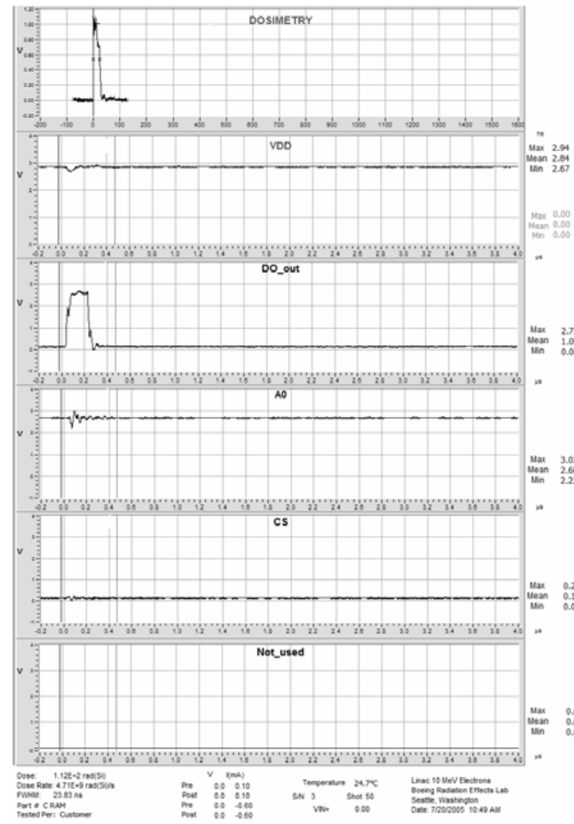

Figure 6. 4M C-RAM Output Transient (0 to 1)

This output transient, a 0 to 1 pulse on a monitored data bit, was determined to be the result of a collapse of the reference voltage to the sense amp relative to VDD. In normal operation, this reference voltage input (utilized in margin testing of the programmed memory bits) would be tied to VDD on the circuit board.

Additional decoupling was added to the test board for the reference voltage supply prior to PD Survive testing. As a result, the analysis of the transient error observed during upset testing was confirmed.

D. Prompt Dose Survival

1) Prompt Dose Survival Evaluation

Burnout testing was performed using the Hermes III Flash X-ray located at the Sandia National Laboratory (Bremsstrahlung mode).

To minimize the possibility of non-dose related damage during exposure, the test card was placed in a grounded noise cassette (provided by Sandia). This cassette is necessary to prevent coupling of electromagnetic noise into the test fixture which could cause non-radiation induced damage. The test flow follows.

(1) Pre-exposure functional verification of CRAM

(2) Increase VDD to VDD + 20%

(3) Write all "1" memory pattern prior to exposure and verify

(4) Enable the device and all outputs

(5) Expose sample and record VDD supply current to check for latch-up (record pre- and post readings for each exposure)

(6) Post exposure, perform address uniqueness test to check for burn-out damage

(7) If damage is detected, that particular sample will be retained for post failure analysis

Throughout the test, pre- and post VDD, IDD, and exposure dosimetry was recorded.

2) *Prompt Dose Survival Results*

No burnout or destructive effects were observed up to a 1E12 dose. In addition, "operate through" (no permanent bit errors) capability was maintained through 1E12.

V. Summary

During this stage of a multi-year research program, BAE SYSTEMS and Ovonyx have designed, fabricated and begun testing of a 4Mb non volatile chalcogenide random access memory (C-RAM). Initial characterization of the first pass design of the 4M C-RAM is nearing completion. Results are positive with some wafers having >99.9% good bits/die. Radiation testing is ongoing and will be completed in time to support the release of the second pass. A second pass of the design is under way to support enhanced temperature range and to reflect any changes needed from test results of the first pass. The second pass 4M C-RAM will be fabricated in late 2005 and qualification will begin in 2Q06.

VI. Acknowledgment

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